Communications & Computing Newsletter: Q3 2016

Everything You Need to Know About Hitless I/O

Designers of high availability servers, communications gateways and base stations can't compromise on operational uptime. They need to be up and running all day, every day. As a result, these systems are expressly designed to handle software updates in background without interrupting normal system operation. But how do designers update the PLDs used to manage board hardware functions and perform basic housekeeping tasks without power cycling to transfer new hardware configuration data stored in Flash memory to on-chip SRAM? A new hitless I/O feature built into Lattice's MachXO2™ and MachXO3™ PLDs promises to solve this problem by enabling zero-downtime updates. Find the answers to all your questions about this exciting new capability, including how this innovative technology works, what design resources are available, and all relevant documentation on Lattice Semiconductor's new Hitless I/O web page.

IDF Attendees Check Out Lattice's MachXO3LF

The Intel Developers' Forum (IDF) in San Francisco last month proved to be highly educational. Design and test engineers from the communications, server and storage industries came by Lattice's booth to learn more about the enhanced features in the MachXO3LF FPGA. Of particular interest was the device's exciting new Hitless I/O capability which allows users to replace PLD code without interrupting system operations. Visitors also liked the MachXO3LF's new analog I/O features, as well as its ability to directly interface to 1V I/O signals without wasting other 3.3V or 2.5V pins. Engineers also learned the device can do far more than simply function as the main control PLD including applications in hard disk/NMV backplanes, security, HBA boards for out-of-bandwidth signal integration, LED drivers in Riser cards, and maxing and matching of a TMP interface. Learn more here.

Build Better Board Power Management Architectures

Implementing highly efficient power management architectures in today's increasingly complex board designs is no small task. As designers move to higher performance devices in ever-shrinking board footprints, many of the techniques they have relied on in the past no longer apply. In a series of six blog posts, Lattice's Shyam Chandra reviews many of the tradeoffs you will face and offers some helpful tips and strategies to optimize power management in your design. Read the latest blog entryhere.

We're Here for You

Want to keep up-to-date on the latest developments in the industry and learn more about Lattice's smart connectivity portfolio? Lattice's on-line resources offer a wealth of information. Follow us on Twitter, Facebook, LinkedIn andYouTube, and read our bi-weekly blogs for the latest news.

Lattice Semiconductor, 111 SW 5th, Suite 700, Portland, OR 97204

Follow us: